

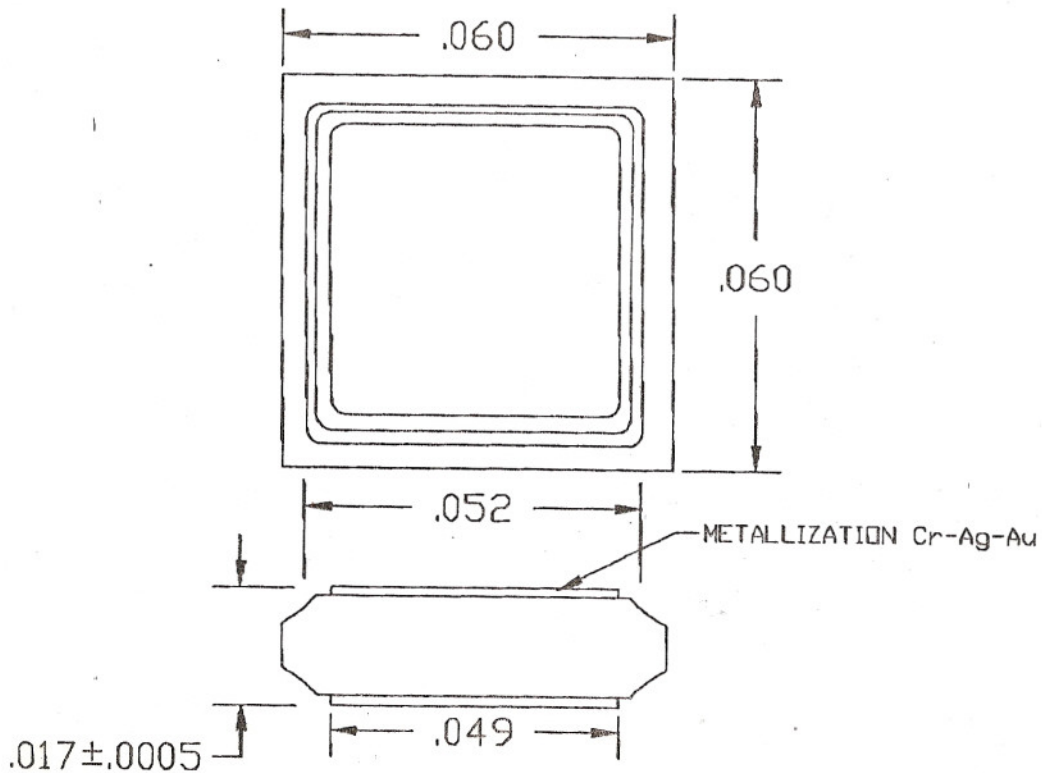


# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Topside Metal: Cr/Ag/Au**

**Backside: Cr/Ag/Au**

**Backside Potential: -**

**Mask Ref: Issue 1**

**Bond Pads: .004" min.**

**APPROVED BY: CD**  
**MFG: Microsemi Corp.**

**DIE SIZE: .060" x .060"**  
**THICKNESS: .017"**

**DATE: 7/24/02**  
**P/N: DZ000121A**